

08/632298

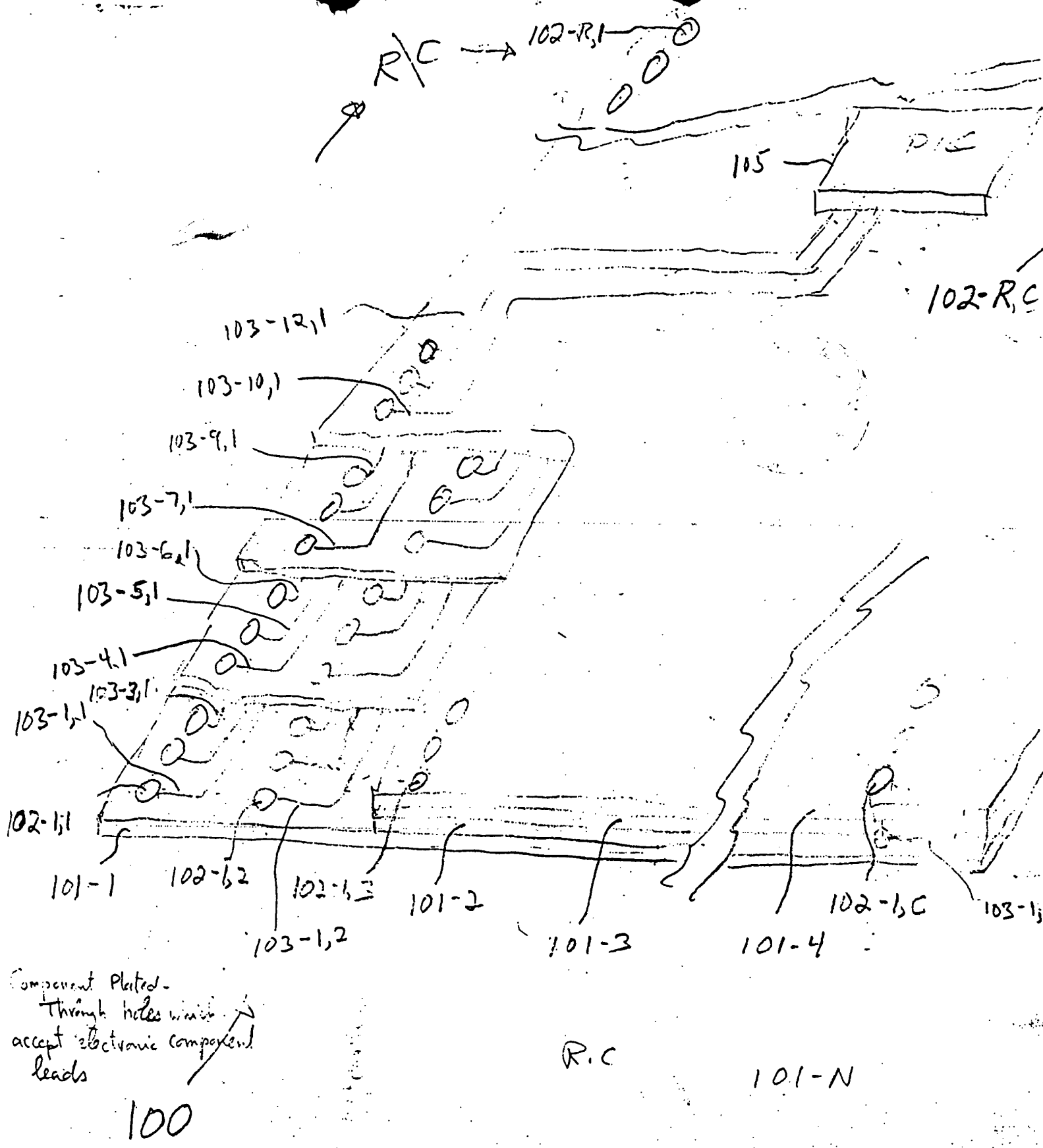


FIGURE 1a

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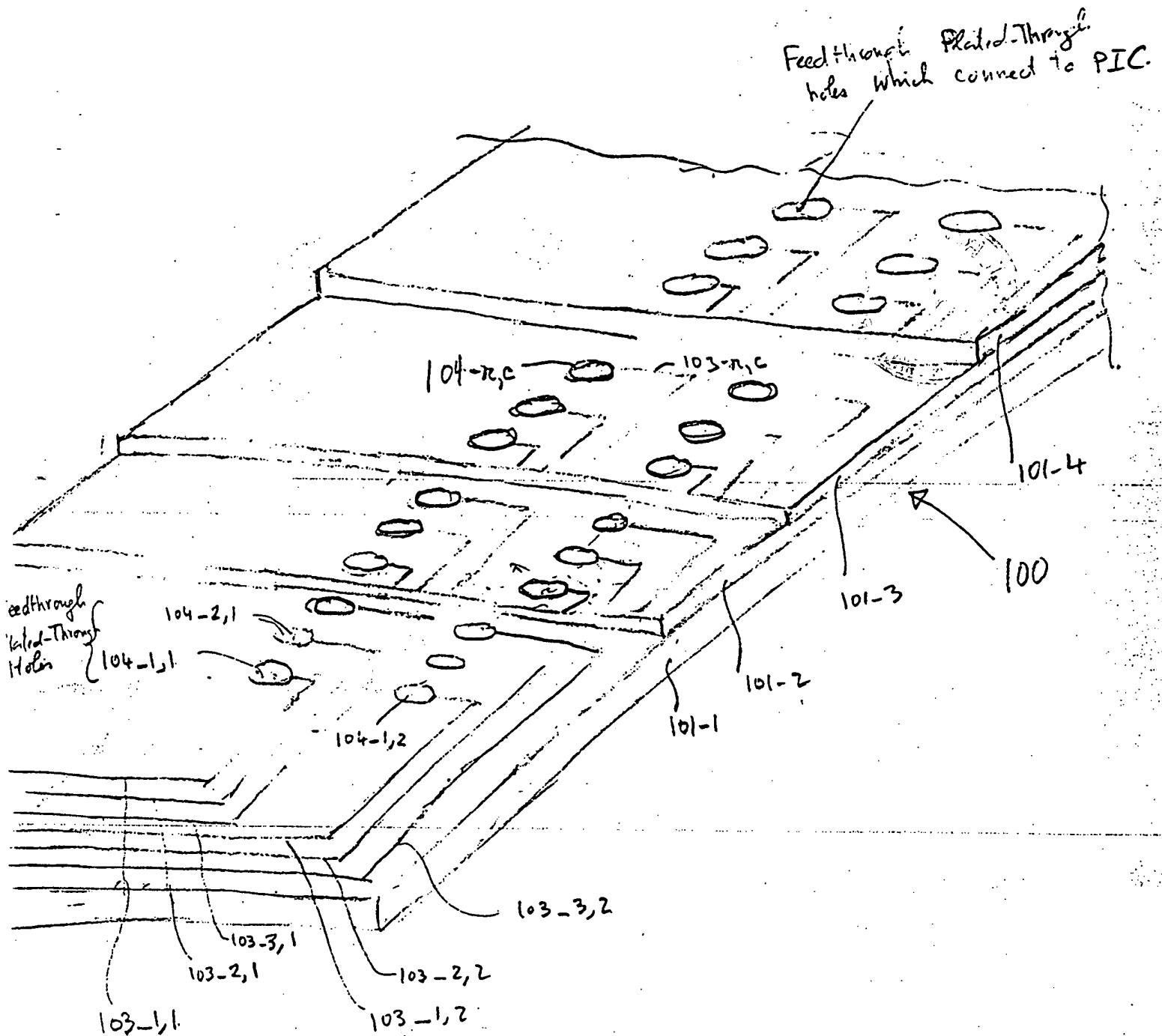


FIGURE 18

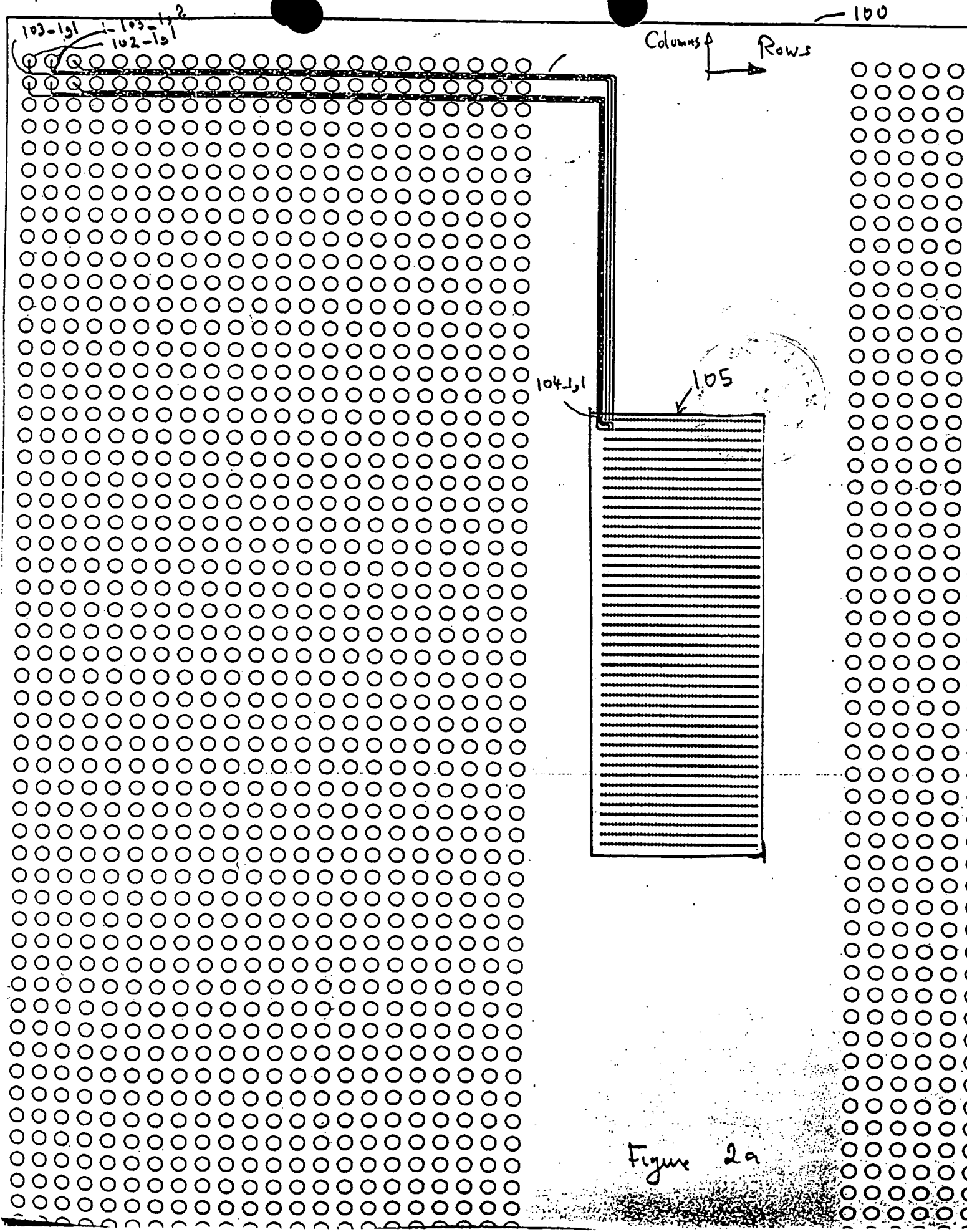


Figure 2a

03/632298
100

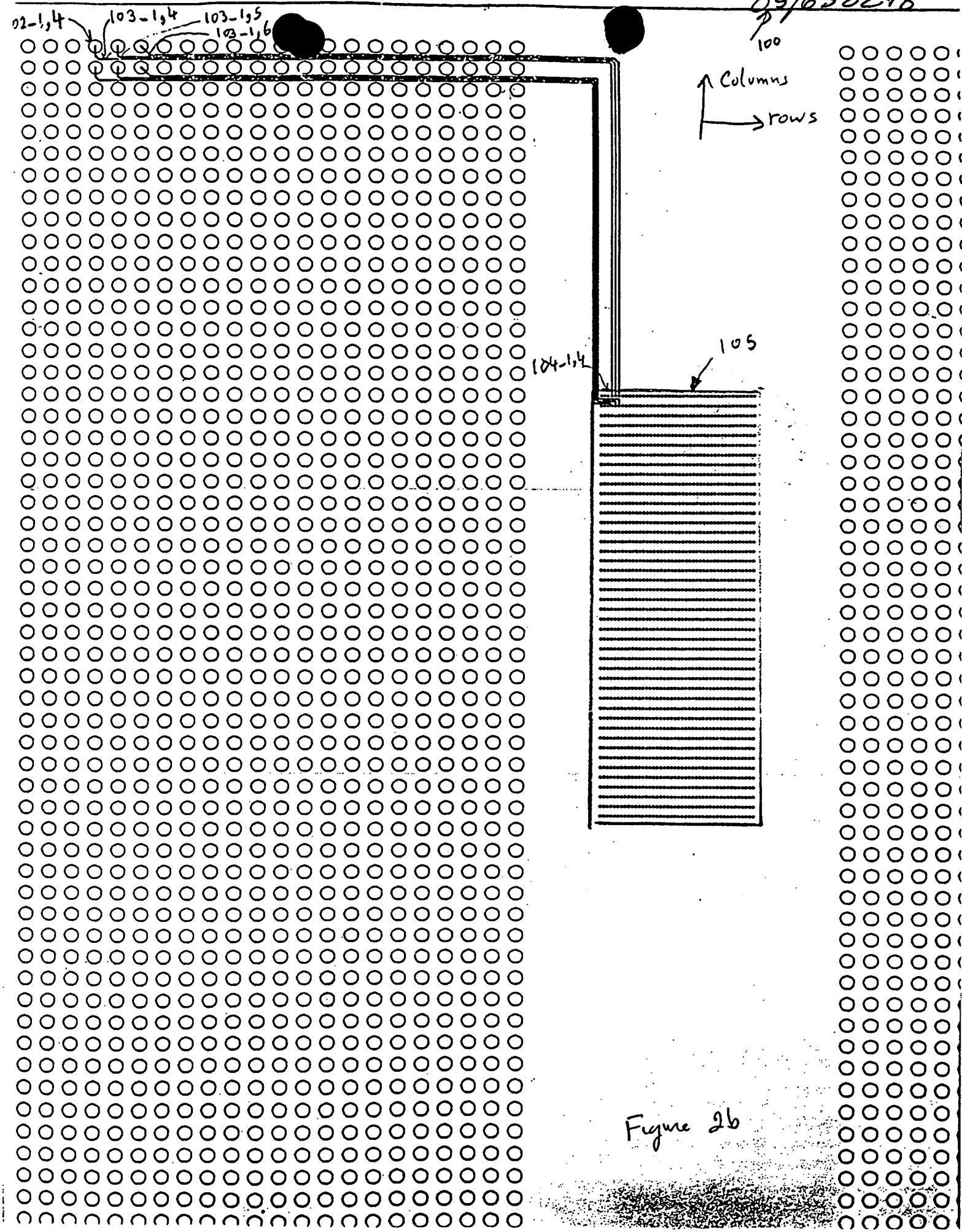
02-1,4
103-1,4
103-1,5
103-1,6

Columns
Rows

104-1,4

105

Figure 2b



09/032298
100

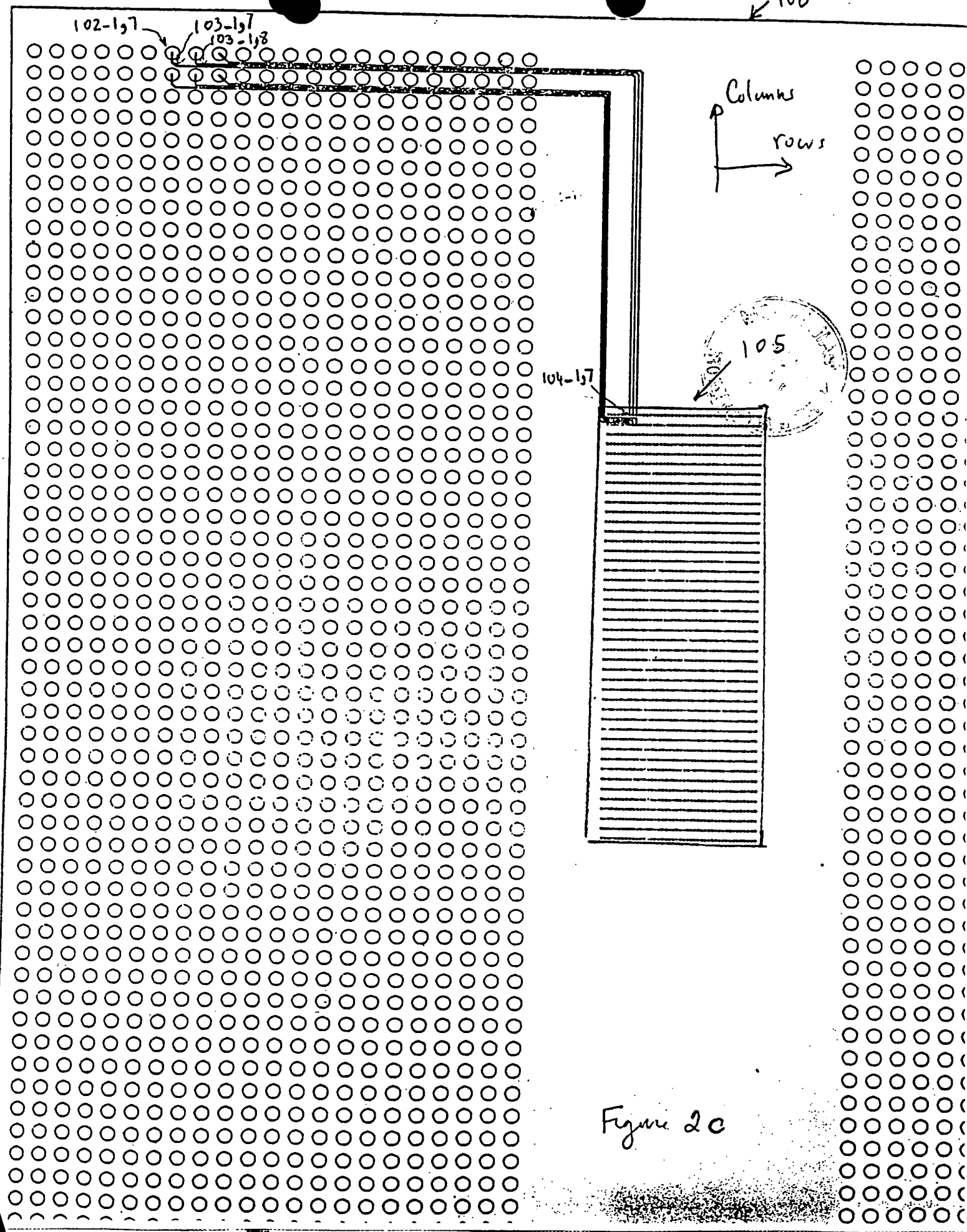


Figure 2c

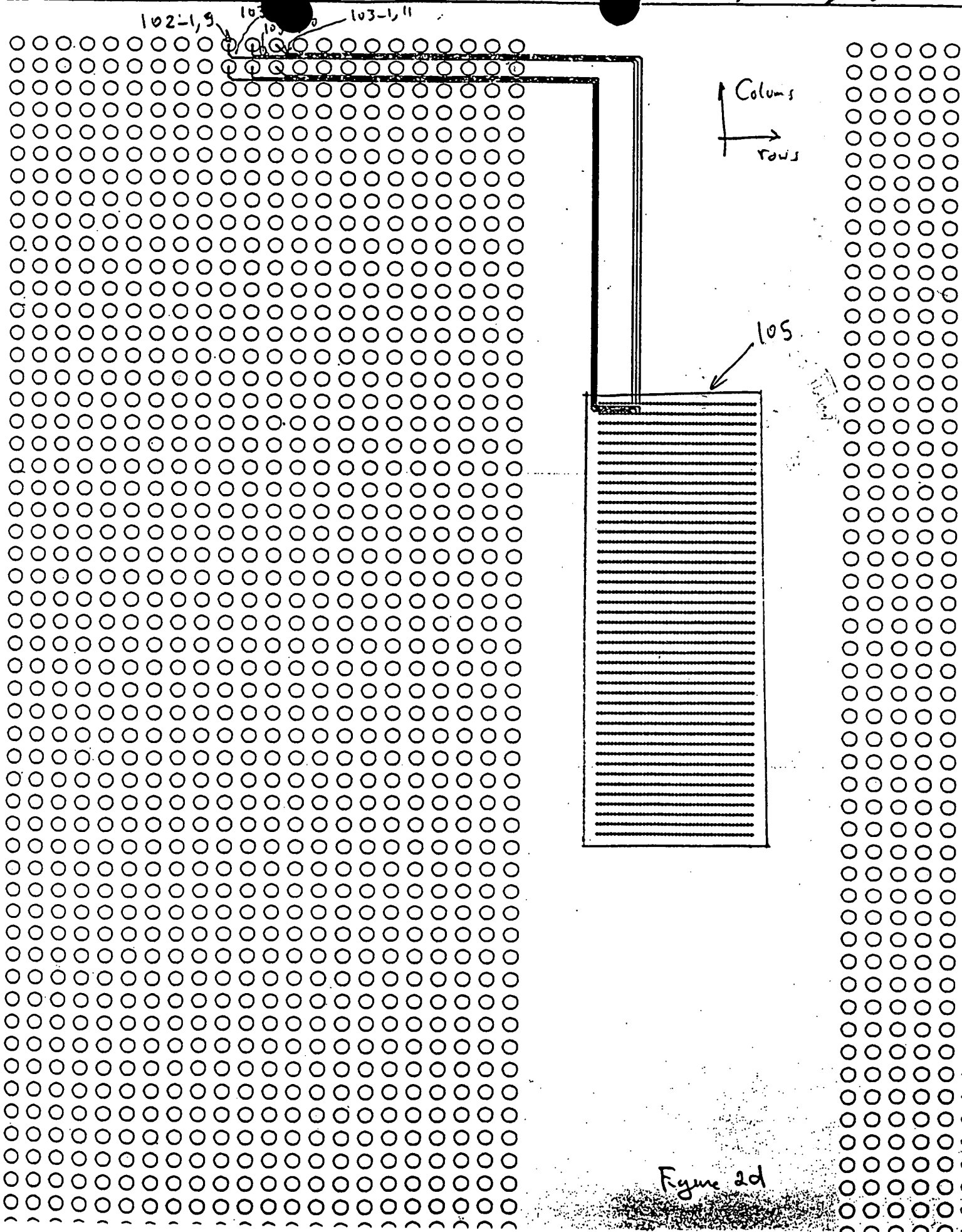


Figure 2d

GLOBAL INTERCONNECT ARCHITECTURE

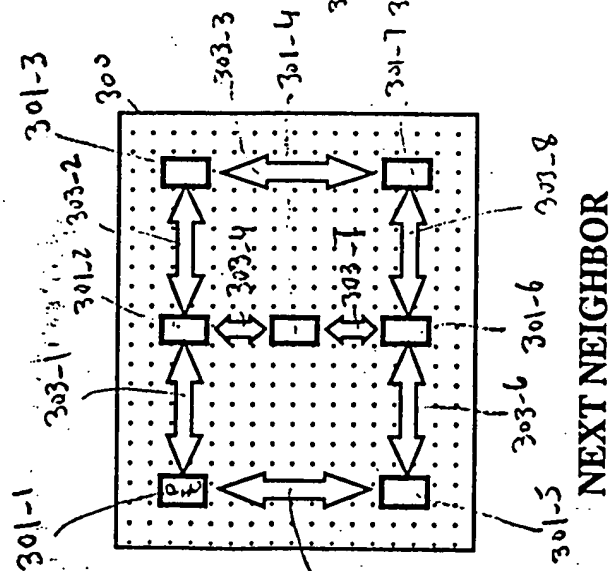


Figure 3a

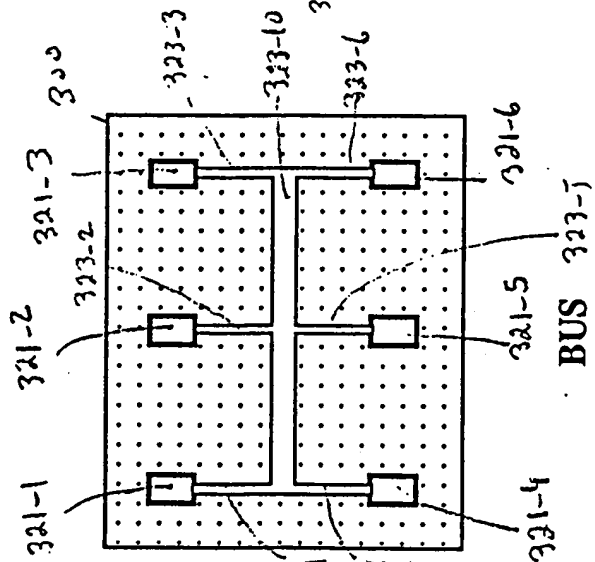


Figure 3c

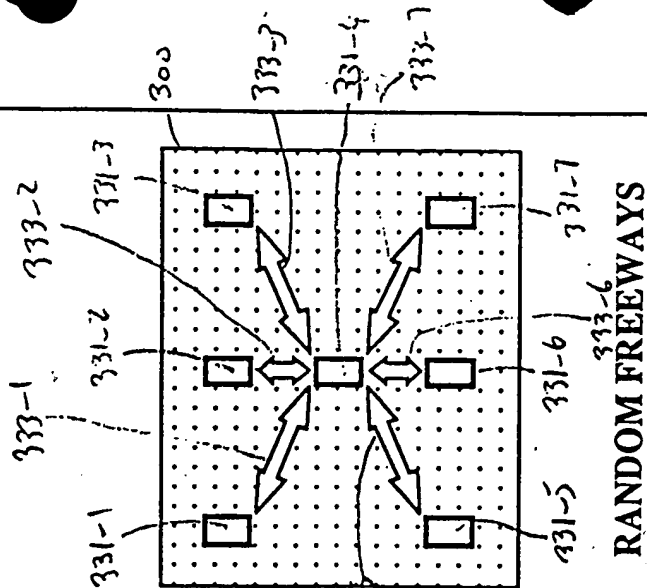


Figure 3d

Hierarchy of Global Interconnects
~~FREEWAY SYSTEM~~
Next Neighbour

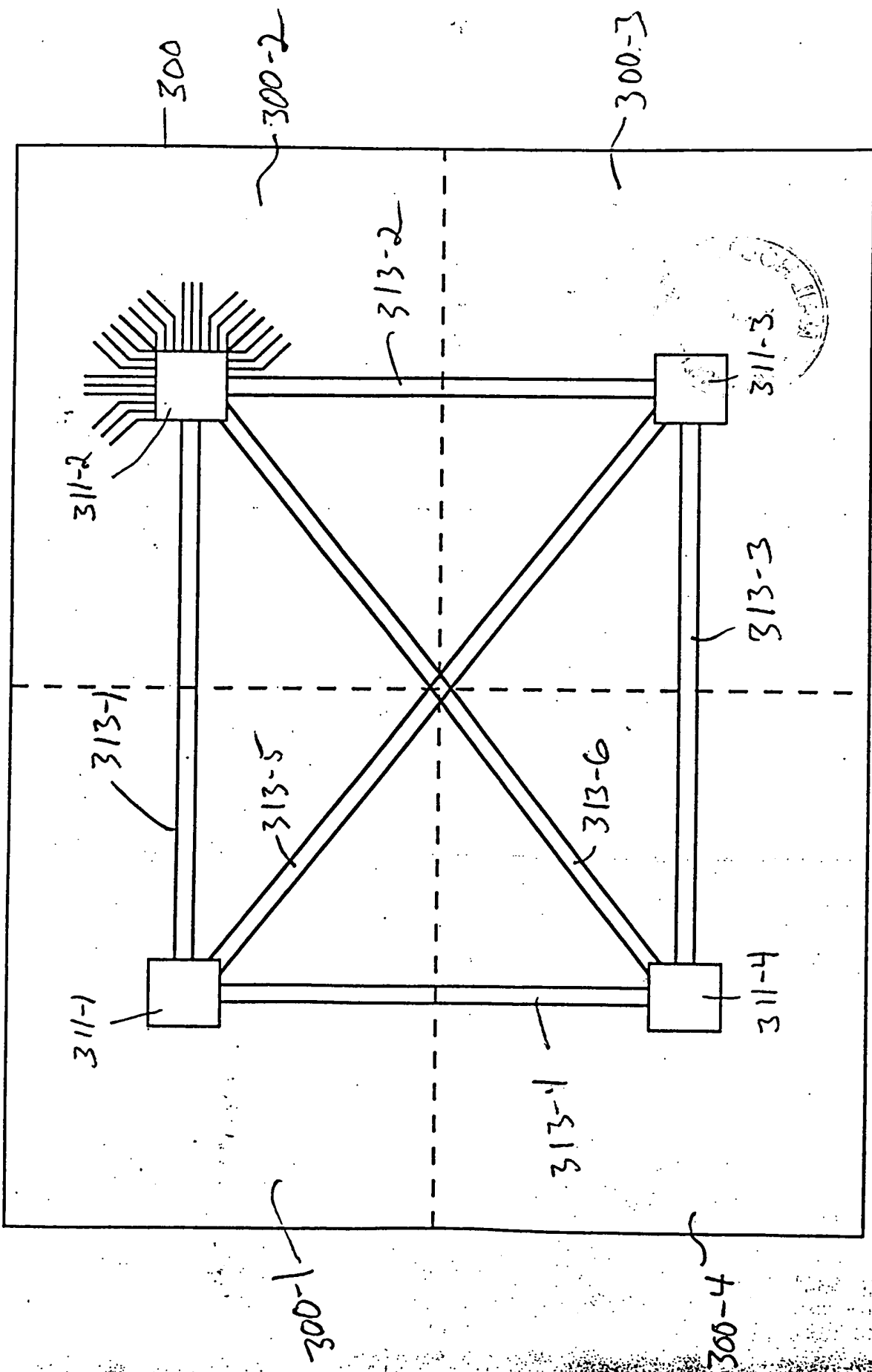


Figure 3b

Control and TESTPORT/DIAGNOSTIC TOOL

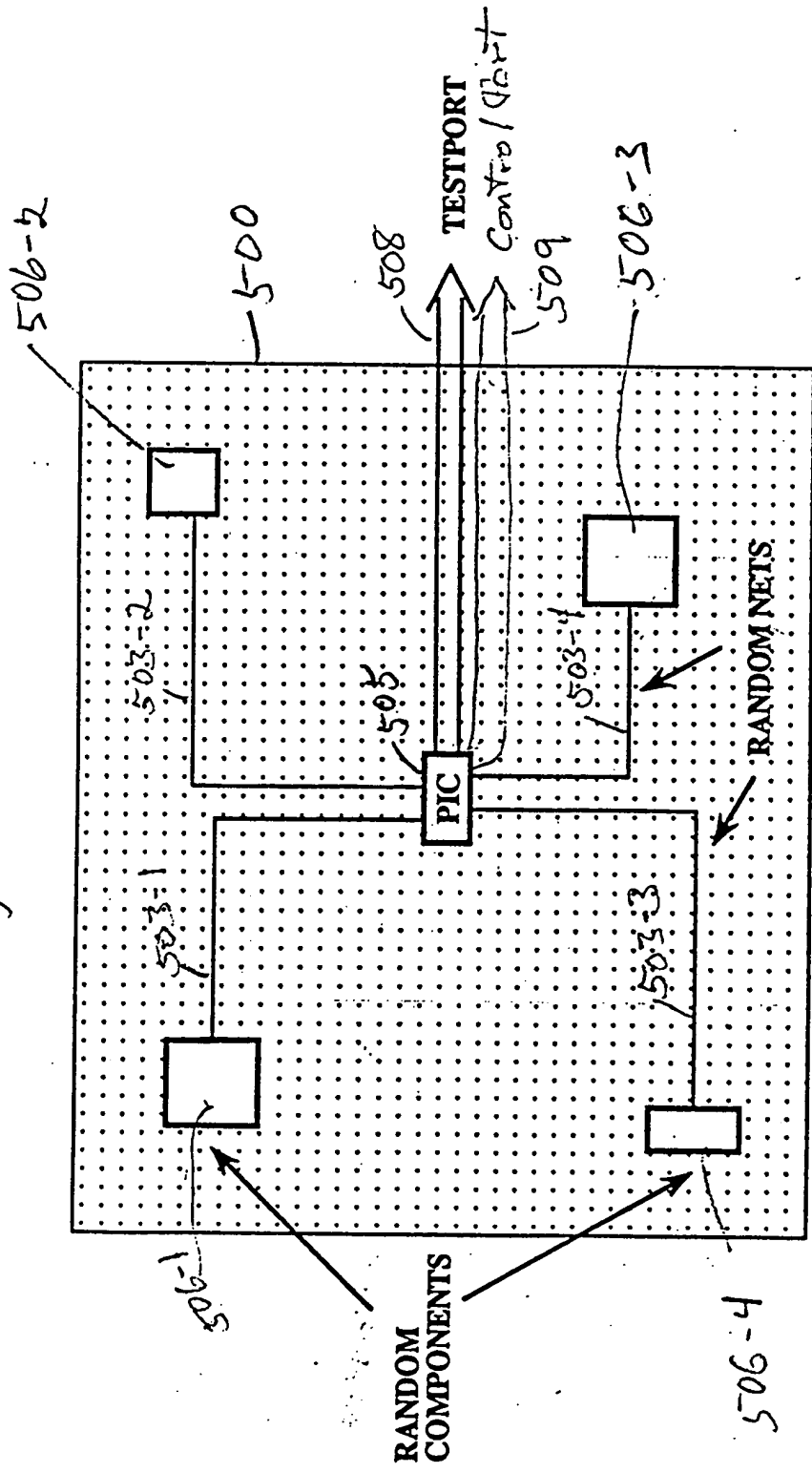


FIGURE 5

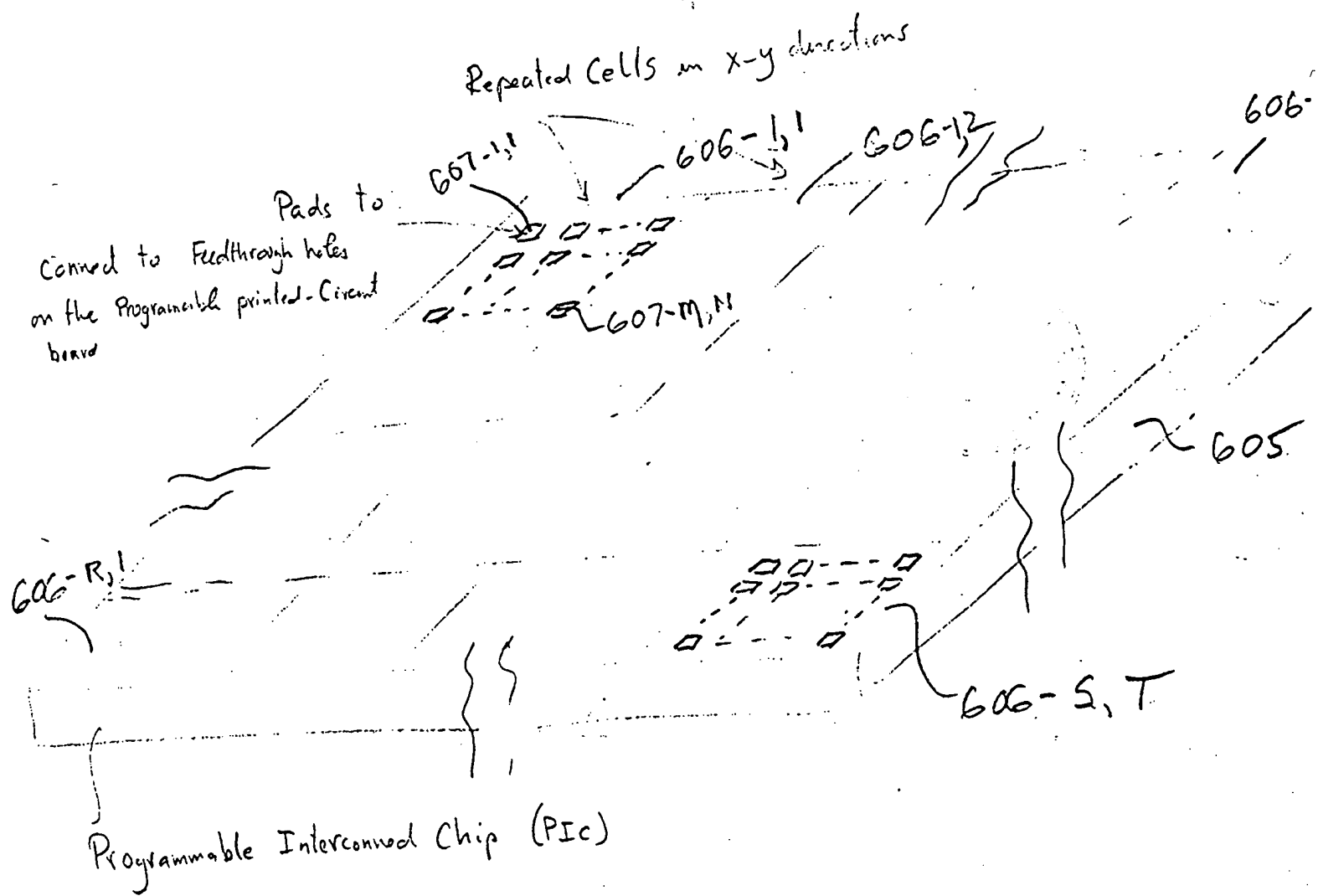
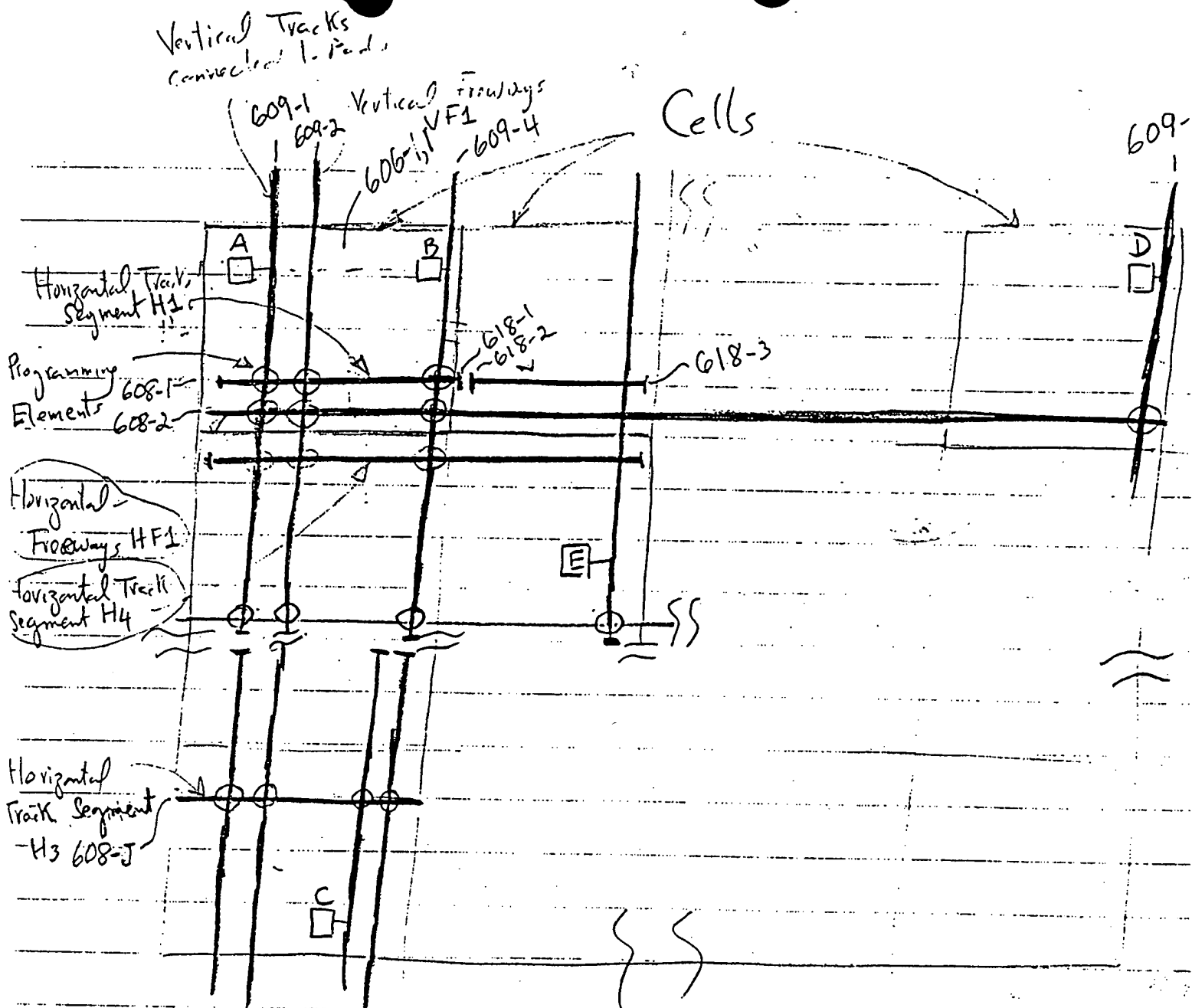


FIGURE 6a



To connect A to B program elements at Intersects (A-H1) and (H1-B)

" A to D " " " " (A-HF1) and (HF1-D)

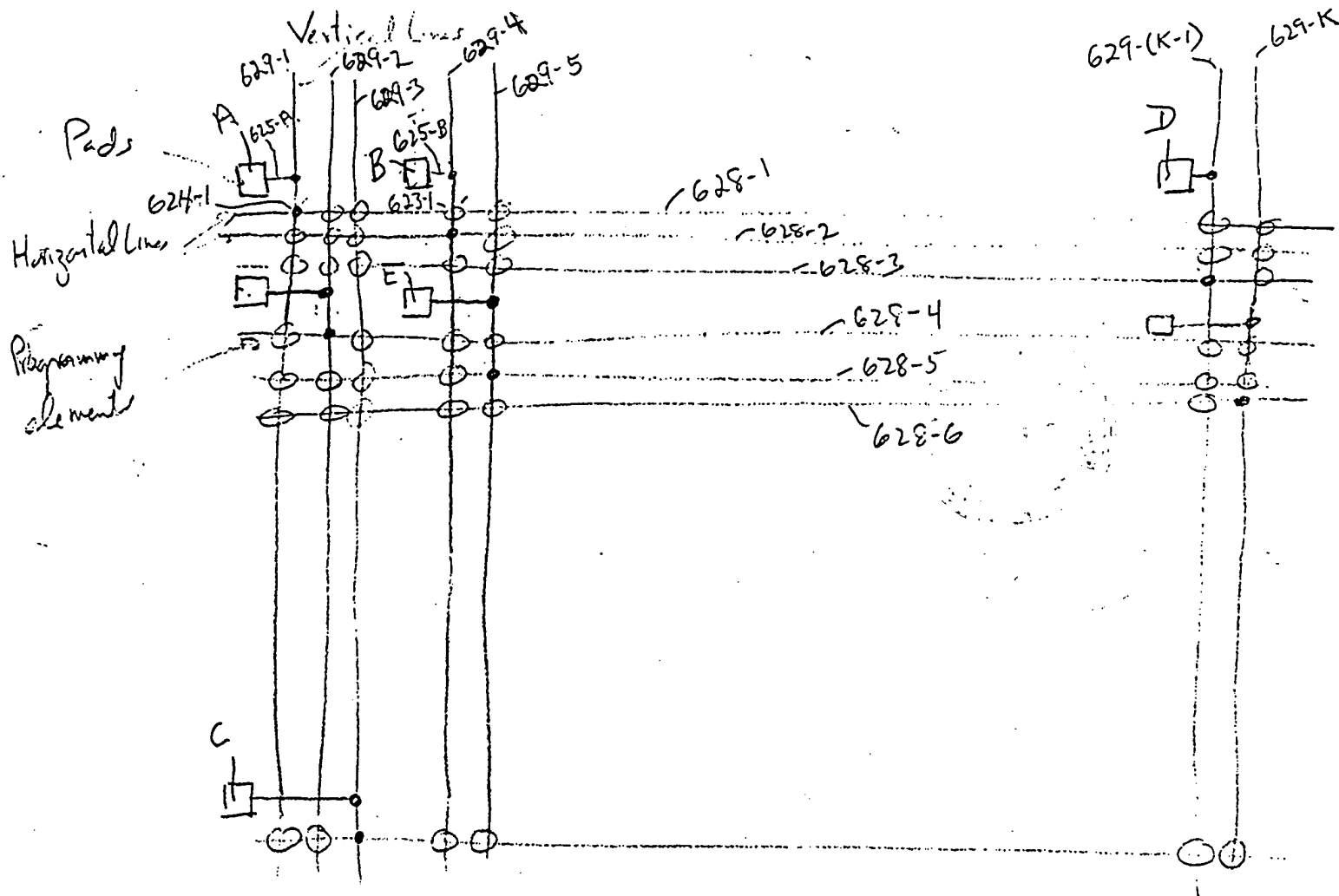
" A to C " " " " (A-H1), (H1-VF1), (VF1-H3) and (H3-C)

" A to E " " " " (A-H4) and (H4-E)

Divided Cross-Point Switch-Matrix Array of the PIC

FIGURE 6B

Single Crosspoint Switch-Matrix way of PIC

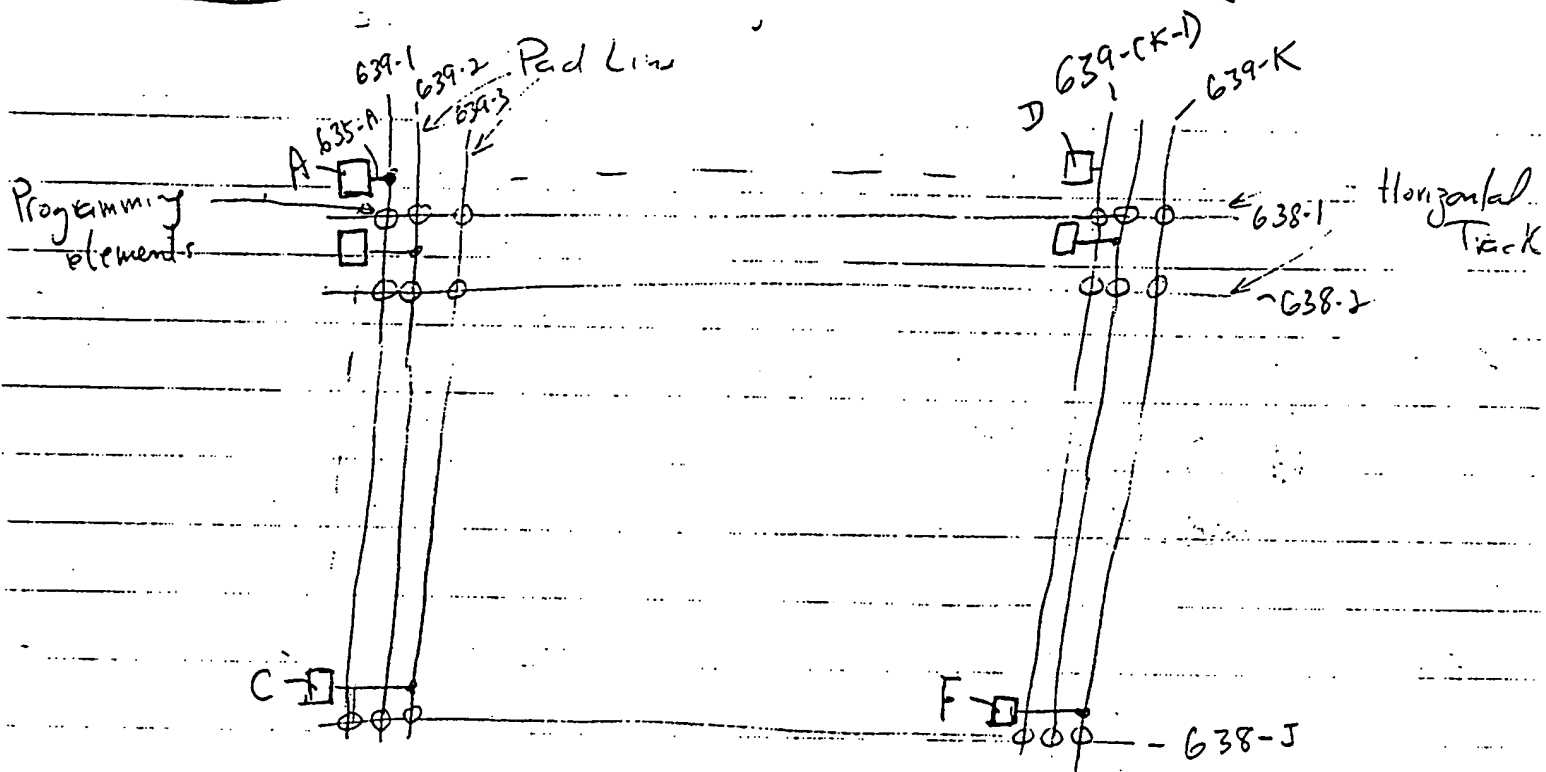


- Each pad connects to a vertical line.
- Each vertical is connected to a horizontal lines
- Connection of one pad to another include one programming element
- Inefficient as number of pads become large (eg 100 - 300)
- Total number of programming elements = $(N_{\text{of Pads}})^2$

FIGURE 6C

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Single Cross-Point Switch - Matrix Array of PIC

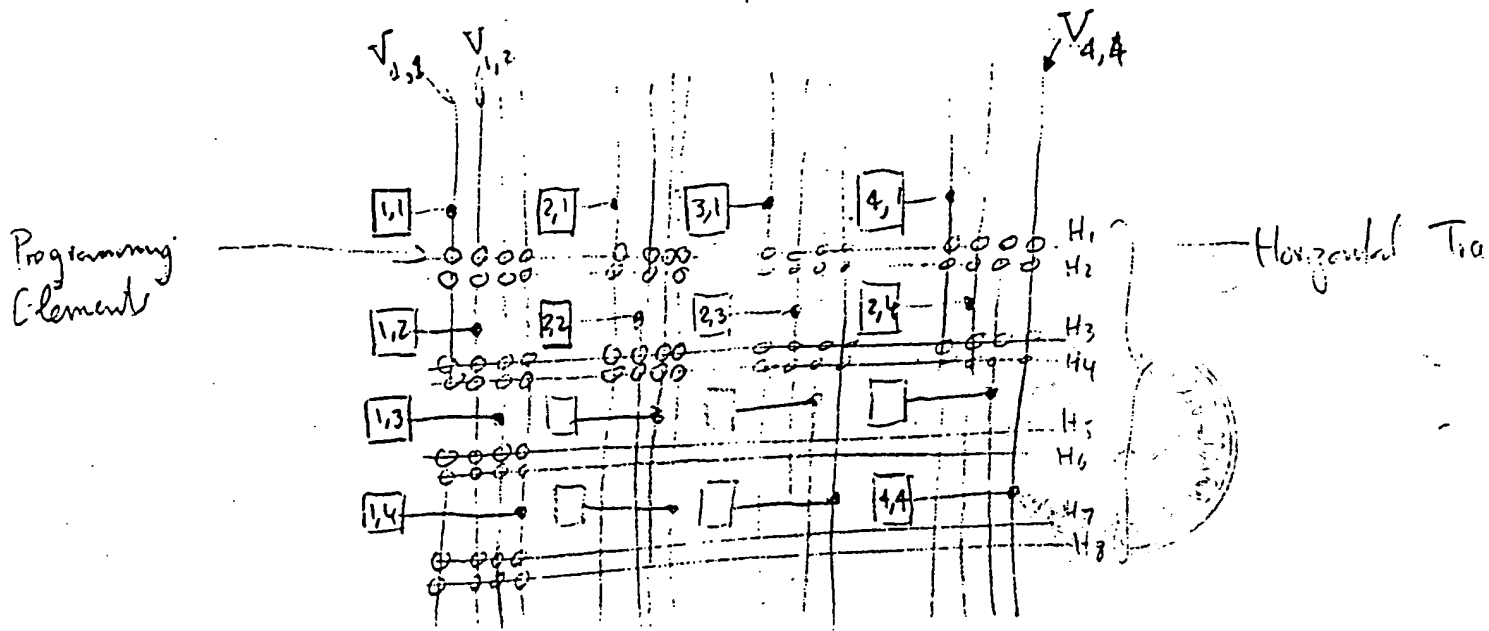


- Each pad connected to a vertical line
- Number of horizontal lines $\leq \frac{1}{2}$ number of vertical lines
- Connection of one pad to another include two programming elements
- Number of programming elements $\leq \frac{1}{2} (\text{Number of pads})^2$
- Inefficient as number of pads become large (For example above 200-500)

FIGURE 6d

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Vertical Tracks



Single Cross-point Switch-Matrix Array For 16 pads

To connect pad (1,1) to pad (4,1)

Program elements at Intersects of $(V_{1,1} - H_1)$ and $(H_1 - V_{4,1})$

To connect pad (1,2) to pad (4,4)

Program element at Intersects of $(V_{1,2} - H_3)$ and $(H_3 - V_{4,4})$

FIGURE 6e

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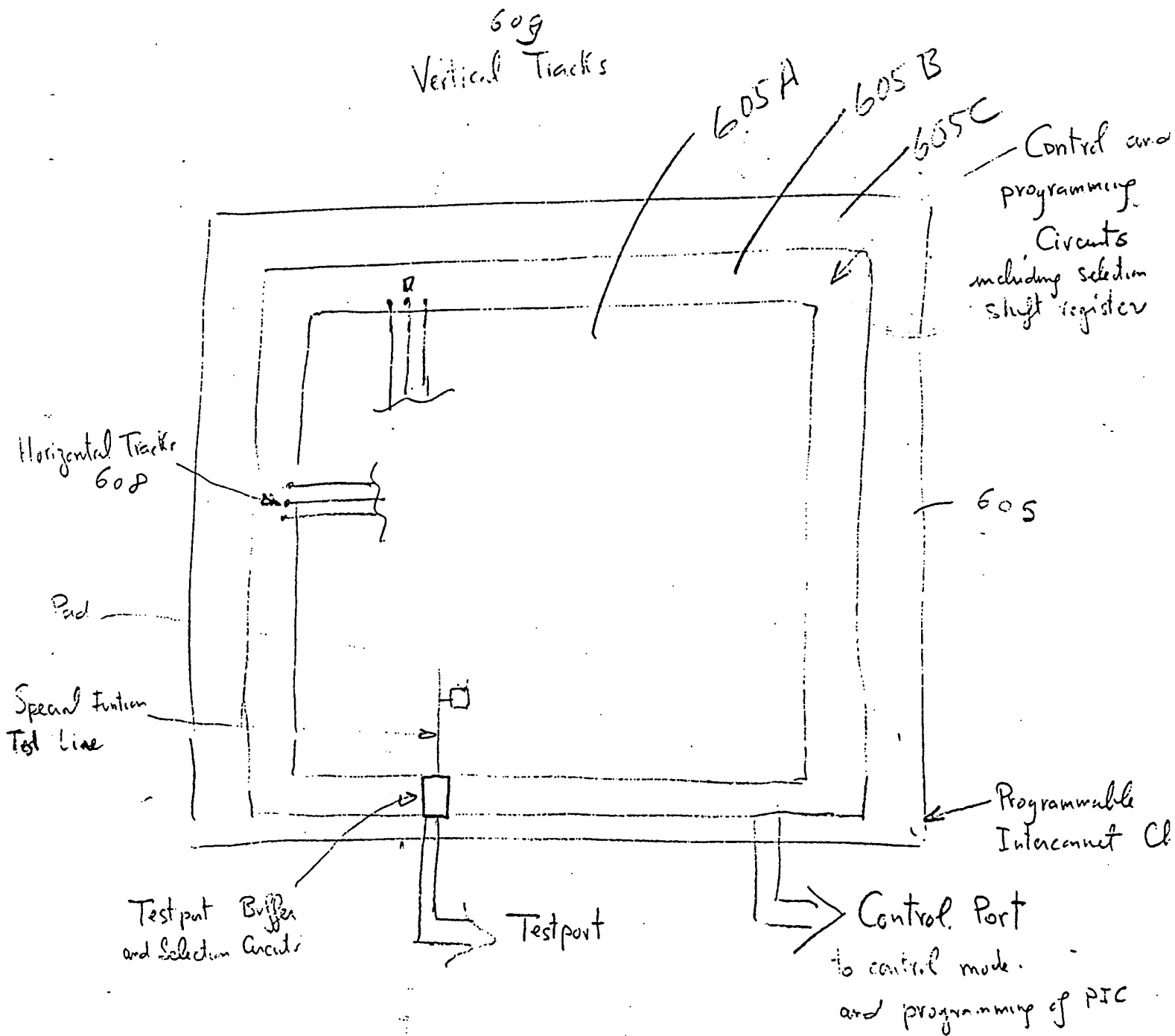
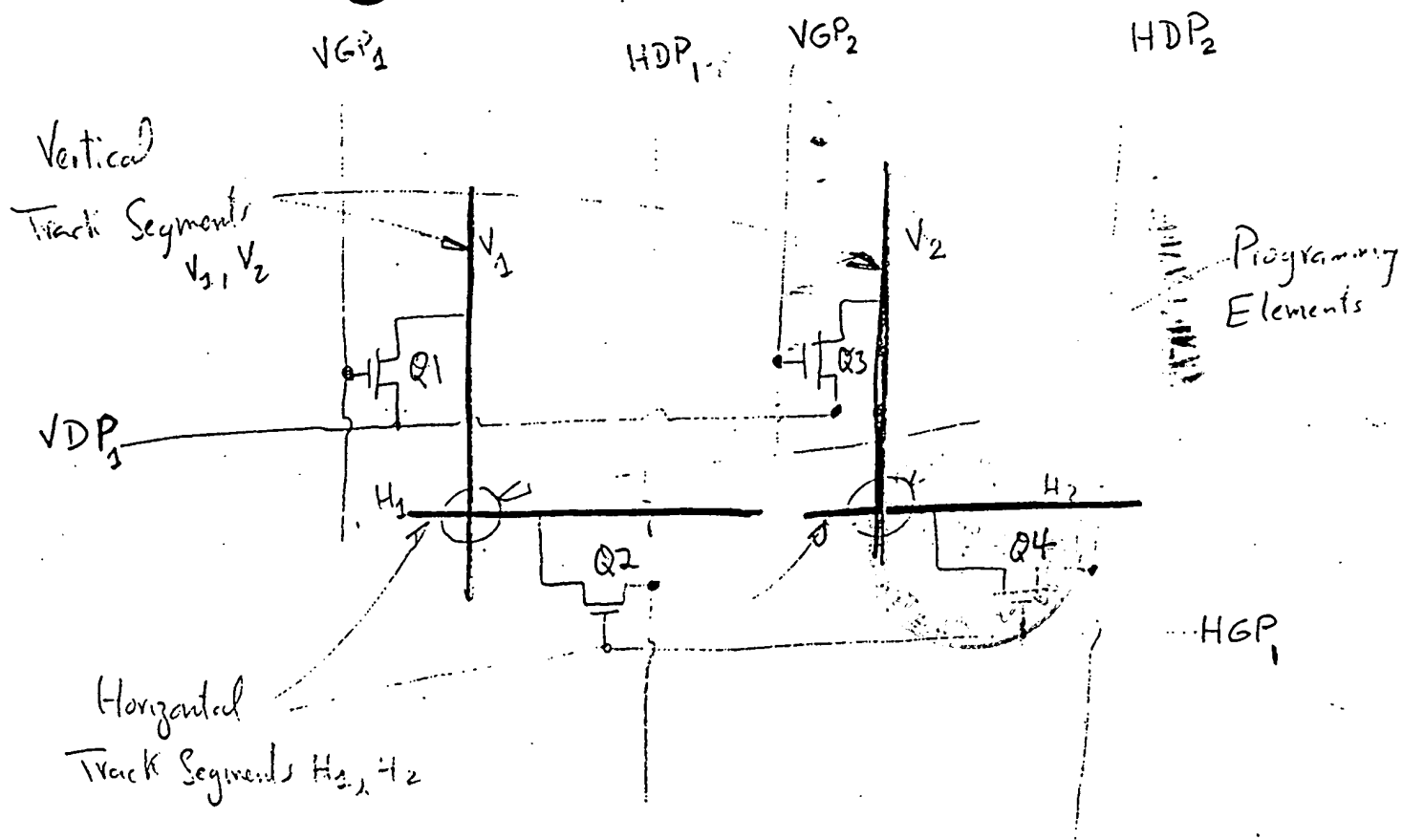


FIGURE 7a

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Programming Scheme to select Horizontal and vertical segments in the PIC with only two transistor in Programming circuit path to allow current to reach hundreds of mAmps.

To program H_1 to V_1 , Take $VGP_1 = V_{GH}$, $VGP_2 = 0$, $VDP_1 = V$
 $HGP_1 = V_{GH}$, $HDP_1 = 0$, $HDP_2 = 0$

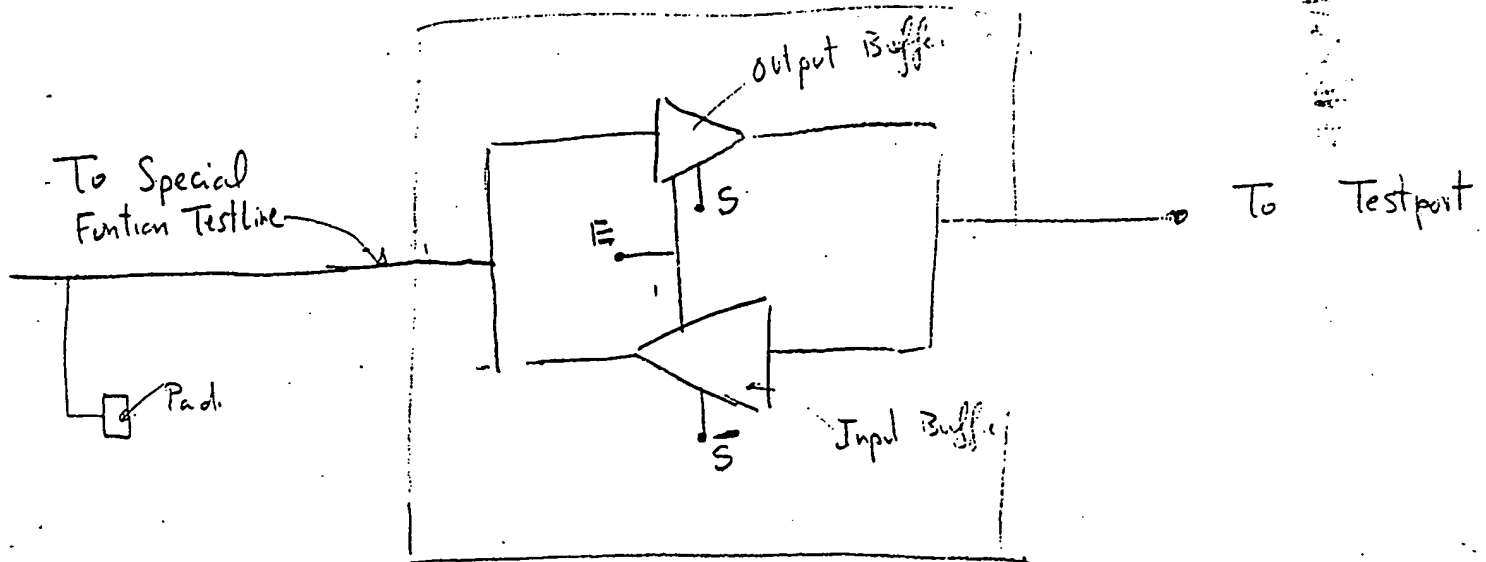
Where V_{pp} is the programming voltage ~ 15 to 50 Volts

V_{GH} is larger than V_{pp} by transistor threshold voltage ~ 1.8 to 5.3 V

Only Programming element at Intersect of track segments H_1 and V_1 see full programming voltage V_{pp}

FIGURE 72

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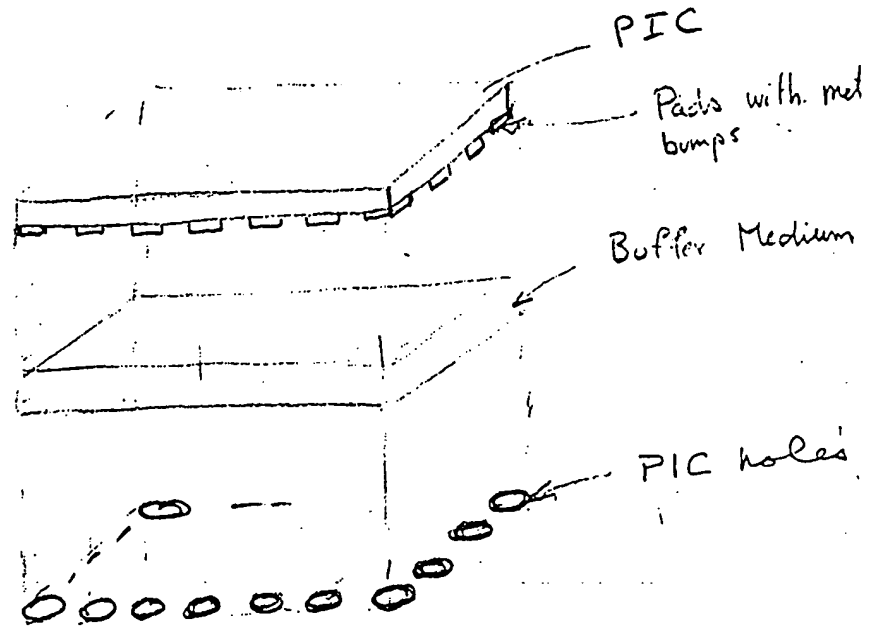
S selects output or input buffer

E selects the pad to connect to test port

FIGURE 7c

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Printed-Circuit board
Surface



Buffer Medium ① Elastomeric material made of polymer with z-axis conductors
5-100 mils thickness

② Carrier of Button springs

FIGURE 2A

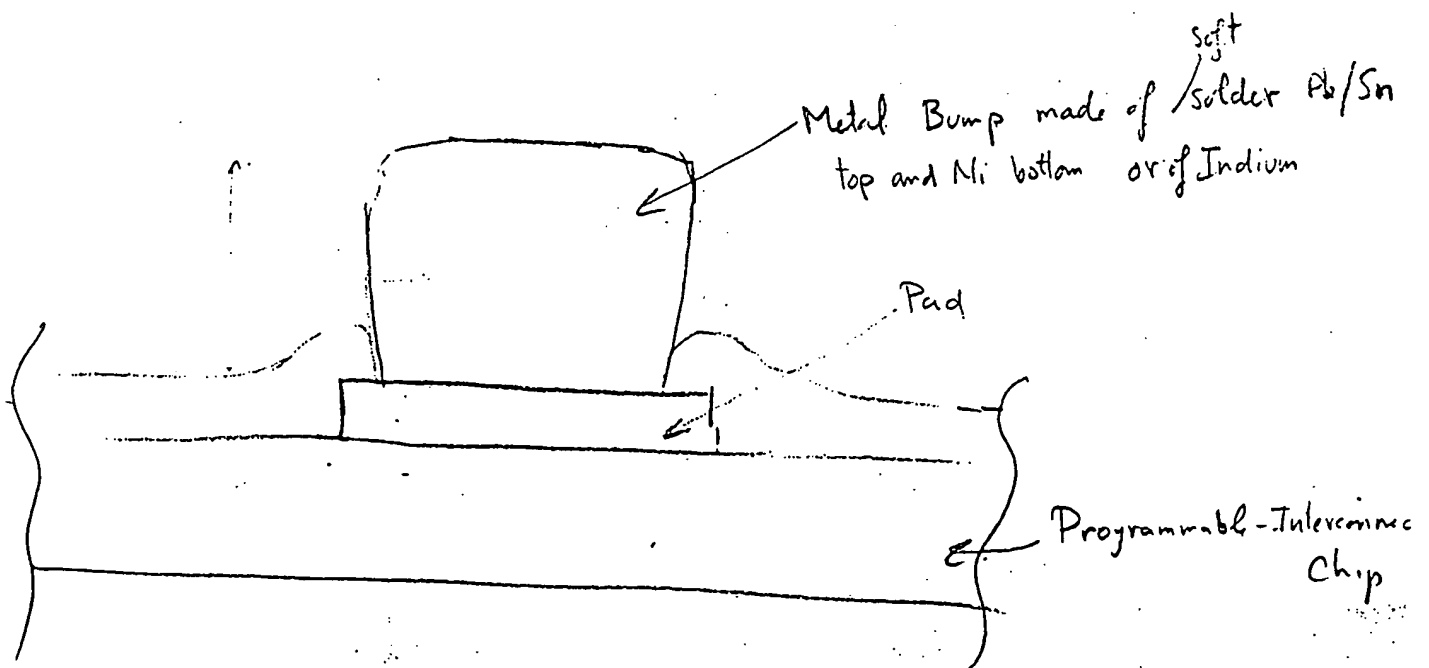
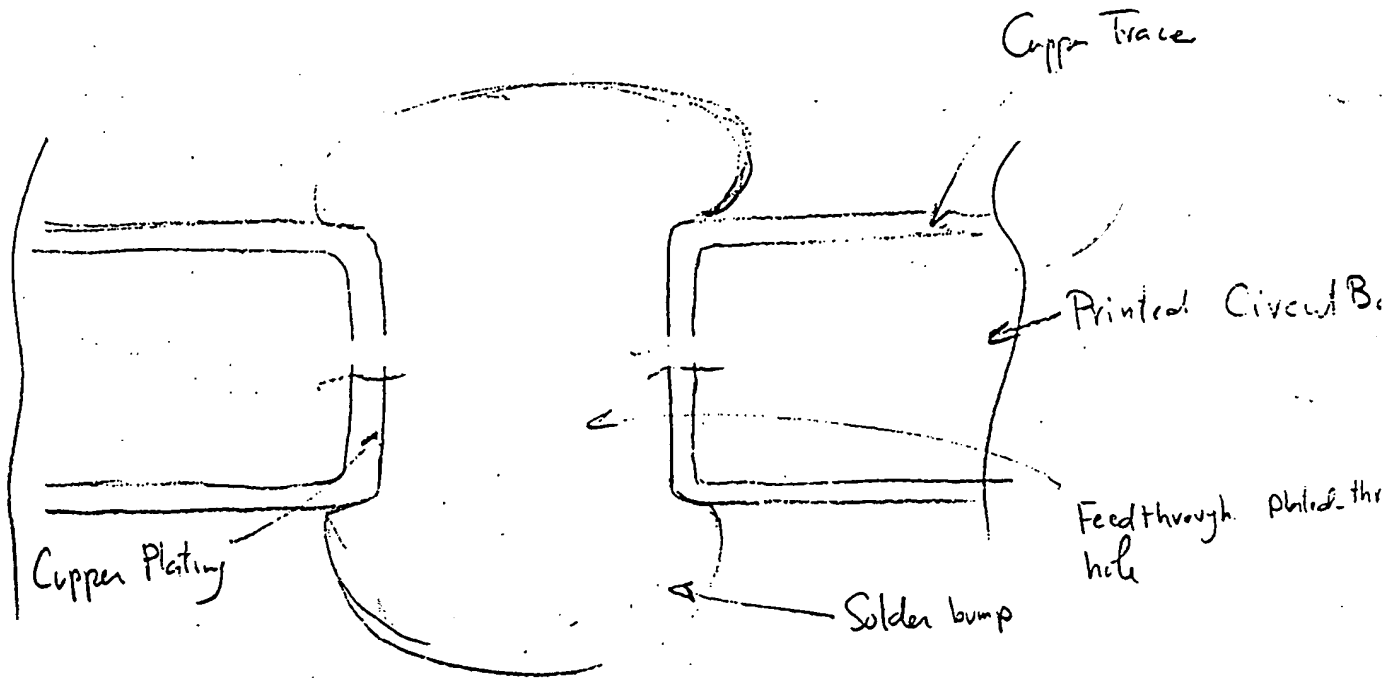


FIGURE 86

M-1007

START

CREATE COMPUTER MODEL OF STANDARD PRINTED CIRCUIT BOARD HAVING (A) COMPONENT CONTACTS FOR RECEIVING THE ELECTRICAL LEADS OF ELECTRONIC COMPONENTS, (B) PIC CONTACTS FOR RECEIVING THE ELECTRICAL LEADS OF ONE OR MORE PROGRAMMABLE INTERCONNECT CHIPS, AND (C) CONDUCTIVE TRACES FOR CONNECTING THE COMPONENT CONTACTS TO THE PIC CONTACTS

SELECT ELECTRONIC COMPONENTS THAT FORM A SYSTEM TO IMPLEMENT A DESIRED FUNCTION, AND DETERMINE INITIAL INTERCONNECTION OF SELECTED COMPONENTS

SIMULATE PLACEMENT AND ROUTING OF THE COMPONENTS ON THE BOARD

MODIFY PLACEMENT OF THE COMPONENTS

SIMULATE (A) INTERCONNECTION OF THE COMPONENTS IN DESIRED FASHION AND (B) CONFIGURATION OF THE PIC(S) USED FOR THE INTERCONNECTION

MODIFY PIC INTERCONNECTION CONFIGURATION

SIMULATE SYSTEM ELECTRICAL PERFORMANCE WITH THE COMPONENTS SO INTERCONNECTED

DETERMINE RESULTING SYSTEM PERFORMANCE AND SYSTEM CHARACTERISTICS

COMPARE DESIRED SYSTEM CHARACTERISTICS AND FUNCTIONAL PERFORMANCE TO SIMULATED SYSTEM CHARACTERISTICS AND FUNCTIONAL PERFORMANCE

YES
ADEQUATE?
NO
FINISH

FIGURE 9